IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings of claims in the application:

1. (Currently Amended) A semiconductor device comprising:

a semiconductor substrate;

a MOSFET formed on the substrate;

a signal input pad connected to a gate of the MOSFET, said signal input pad receiving an input signal for the MOSFET;

a high concentration impurity diffused region located beneath the signal input pad and at a surface part of the semiconductor substrate;

an interconnection connected to the high concentration impurity diffused region, said interconnection being electrically isolated from said signal input pad; and

a low resistance layer provided on the upper surface of the high concentration impurity diffused region and directly under the signal input pad, this low resistance layer acting as a shield,

wherein the high concentration impurity diffused region is a substrate/well potential take-out region.

2. (Original) The semiconductor device according to claim 1, wherein said high concentration impurity diffused region is enveloped by a device isolation film.

3. (Original) The semiconductor device according to claim 1, wherein said low resistance layer is a metal silicide layer.

4. (Original) The semiconductor device according to claim 1, wherein a potential same as that of the substrate or a well of the MOSFET is applied to the low resistance layer.

5. (Previously Cancelled).

6. (Original) The semiconductor device according to claim 1, wherein a plurality of MOSFETs disposed in comb-like shape on the semiconductor substrate form an amplifier stage.

7. (Currently Amended) A semiconductor device comprising:

a semiconductor substrate;

a MOSFET formed on the substrate;

a signal input pad connected to a gate of the MOSFET, said signal input pad receiving an input signal for the MOSFET;

a high concentration impurity diffused region located below the signal input pad and at a surface part of the semiconductor substrate;

an interconnection connected to the high concentration impurity diffused region, said interconnection being electrically isolated from said signal input pad;

a polysilicon layer provided beneath said signal input pad, said polysilicon layer being connected to the interconnection, and

a low resistance layer provided on the upper surface of the high concentration impurity diffused region and said polysilicon layer this low resistance layer being provided directly under the signal input pad and acting as a shield,

wherein the high concentration impurity diffused region is a substrate/well potential take-out region.

8. (Original) The semiconductor device according to claim 7, wherein said high concentration impurity diffused region is enveloped by a device isolation film and wherein said polysilicon layer is provided on the device isolation layer.

9. (Original) The semiconductor device according to claim 8, wherein said low resistance layer is a metal silicide layer.

10. (Original) The semiconductor device according to claim 7, wherein the low resistance layer is also provided on the polysilicon layer.

11. (Original) The semiconductor device according to claim 7, wherein a potential same as that of the substrate or a well of the MOSFET is applied to the low resistance layer.

12. (Cancelled).

13. (Currently Amended) The semiconductor device according to claim [[1]] 7, wherein a plurality of MOSFETs disposed in comb-like shape on the semiconductor substrate form an amplifier stage.

14. (Withdrawn) A method for manufacturing a semiconductor device comprising the steps of:

forming device isolation layer for defining a device region and a high concentration impurity diffused region;

forming a gate electrode on a surface of the substrate within the device region;

implanting ions in the device region and the high concentration impurity diffused region with the device isolation layers and the gate electrode being as implantation mask;

depositing low resistance layer at least on the upper surface of the high concentration impurity diffused region , this low resistance layer acting as a shield during operation;

depositing an inter-layer insulating film;

forming a first interconnection connected to the gate electrode and a second interconnection connected to the high concentration impurity diffused region on the said inter-layer insulating film, at least the first interconnection being disposed so that it runs above the high concentration impurity diffused region.

15. (Withdrawn) The method according to claim 14, wherein said low resistance layer is metal silicide layer deposited through a salicide process.

16. (Cancelled).

17. (Cancelled).

18. (Currently Amended) The semiconductor device according to claim 1, wherein said signal input pad is ~~locates~~ located above an area of the high concentration impurity diffused region.

19. (Currently Amended) The ~~seminconductor~~ semiconductor device according to claim 7, wherein said signal input pad is ~~locates~~ located above an area of the polysilicon layer.

20. (New) The semiconductor device according to claim 7, wherein said polysilicon layer is provided on a device isolation film which envelopes said high concentration impurity diffused region and wherein said polysilicon is provided beneath said signal input pad.